What Is Claimed Is:

1. A semiconductor device with improved electrostatic discharge (ESD) tolerance, comprising:

a pad on a semiconductor substrate of a first-conductive type;

a finger-type transistor on the semiconductor substrate, comprising:

at least one drain region of a second-conductive type, coupled to the pad;

a plurality of source regions of the second-conductive type, coupled to a power rail; and

a plurality of channel regions formed on the semiconductor substrate, each channel region located between one of the source regions and one of the at least one drain region;

a well stripe of the second-conductive type on the semiconductor substrate, extending in a first direction at an angle to a channel width direction of at least one of the channel regions; and

a doped segment of the first-conductive type in the well stripe, coupled to the pad.

2. The semiconductor device as claimed in claim 1, wherein the angle is around 90°.

3. The semiconductor device as claimed in claim 1, wherein the well stripe is coupled to the pad.

4. The semiconductor device as claimed in claim 3, wherein the well has at least one contact region of the second-conductive type coupled to the pad.

5. The semiconductor device as claimed in claim 4, wherein the contact region is located between the doped segment and the finger-type transistor.

6. The semiconductor device as claimed in claim 4, wherein the doped segment is located between the contact region and the finger-type transistor.

7. The semiconductor device as claimed in claim 4, wherein the contact region is spaced apart from an end of the doped segment.

8. The semiconductor device as claimed in claim 1, wherein the doped segment is formed by a plurality of doped regions of the first conductivity type distributed in the well stripe.

9. The semiconductor device as claimed in claim 1, wherein the well stripe is located between the finger-type transistor and the pad.

10. The semiconductor device as claimed in claim 1, wherein the well stripe is located under the pad.

11. The semiconductor device as claimed in claim 1, wherein the finger-type transistor has gate fingers, each gate finger corresponding to one of the channel regions.

12. The semiconductor device as claimed in claim 11, wherein at least one of the gate fingers is coupled to the power rail.

13. The semiconductor device as claimed in claim 11, wherein at least one of the gate fingers is coupled to a ~~gate~~ signal line.

14. The semiconductor device as claimed in claim 1, wherein the finger-type transistor is a field-oxide transistor, the field-oxide transistor comprises a plurality of isolation segments, and each isolation segment overlaps one of the channel regions.

15. The semiconductor device as claimed in claim 1, wherein the semiconductor device further comprises a pickup ring of the first-conductive type on the semiconductor substrate, the pickup ring coupled to the power rail and extending around the finger-type transistor on three sides.

16. The semiconductor device as claimed in claim 15, wherein the pickup ring surrounds the finger-type transistor and the well stripe.

17. A pad Cell of a semiconductor integrated circuit, comprising:

a pad;

a transistor formed on a substrate of a first conductive type;

a conductor segment positioned between the pad and the transistor for coupling the pad and the transistor;

a well region of a second conductive type formed in the substrate and spaced apart from the transistor; and

a first doped region disposed in the well region;

wherein

the well region is positioned substantially under the conductor segment; and

the first doped region is coupled to the conductor segment.

18. The cell as claimed in claim 17, wherein the first doped region is of the first conductive type.

19. The cell as claimed in claim 18, further comprising a second doped region of the second conductive type disposed in the well region and coupled to the conductor segment.

20. The cell as claimed in claim 19, wherein the first doped region is positioned substantially between the second doped region and the transistor.

21. The cell as claimed in claim 17, wherein the transistor is formed in an active region, the active region is substantially surrounded by an isolation region, and the well region is spaced apart from the active region by less than 20.1um.

22. The cell as claimed in claim 21, wherein the well region is spaced apart from the active region by less than 5.1um.

23. The cell as claimed in claim 22, wherein the well region is spaced apart from the active region by less than 2.1um.